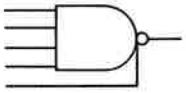
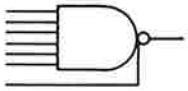
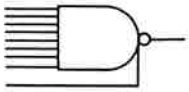
silicon planar epitaxial monolithic integrated electronic blocks for digital systems

packages and type numbers			logic symbol
T	G	Q	
WM 204T	WM 204G	WM 204Q	
WM 214T	WM 214G	WM 214Q	
WM 224T	WM 224G		

design features①

- *fan-out 11 minimum*
- *noise margin 550 mv minimum*
- *switching time 38 ns maximum*
- *power consumption 9.5 mw maximum per gate*
- *only one power supply required*
- *3 packages available:*
  T style modified TO-5
  G style 1/4" x 1/8" FLAT-PAK®
  Q style 1/4" x 1/4" FLAT-PAK

reliability assurance

EVERY unit receives

- high temperature storage bake at +150°C
- 3 cycles of thermal shock −55°C to +150°C
- 20,000 G centrifuge
- gross and helium hermeticity tests

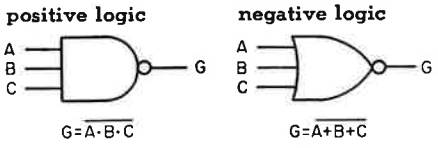
① at V_{cc} = 6.0 v and at 25°C

basic NAND function

The Westinghouse single DTL NAND gates incorporate fan-in capabilities of up to eight. In addition, all of these NAND gates have a common anode point (termed the node) available as an external lead. This permits added fan-in by attachment of additional diodes (see diode arrays WM 207, WM 217 and WM 227). Also, the collectors of two NAND gates may be externally connected to form an AND-OR-NOT function; electrical equivalent circuits describing these NAND gates are shown on page 5.

NAND/NOR function

This gate accomplishes the NAND logic function when the positive logic definition is used. When negative logic is used, the gate accomplishes the NOR logic function. Positive logic results when the more positive of the two voltage levels is defined as the 1-state.



electrical characteristics

absolute maximum ratings①

parameter	symbol	value	units
supply voltage	V_{cc}	+10	volts
input voltage	V_{in}	+10②	volts
node voltage	V_n	+10, −7	volts
output voltage	V_{out}	+7②	volts
ambient storage temperature	T_{stg}	−65 to +175	°C
ambient operating temperature	T_{opg}	−55 to +125	°C

parameter	symbol	limit	values at temperature −55°C	values at temperature +25°C	values at temperature +125°C	units
static electrical characteristics for V_{cc} = +6.0 volts						
total power consumption, 50% duty cycle	P_c	max. typ.	10.5	9.5 7.5	7.5	mw mw
input current, input grounded	I_{in}	max.	2.10	1.80	1.50	ma
input voltage for 0-state output, fan-out of six	$V_{in}/0$	min.	2.10	1.80	1.40	volts
input voltage for 1-state output, fan-out of one	$V_{in}/1$	max.	1.40	1.00	0.60	volts
input diode reverse current at V_{in} = +6.0 volts	I_R	max. typ.		0.01	25.0 1.0	μa μa
output current at the specified $V_{CE(SAT)}$	I_{out}	min. typ.	13.0	20.0 32.0	9.0	ma ma
	$V_{CE(SAT)}$	max.	0.55	0.45	0.35	volts
output cutoff current for V_{CEX} = +6.0 volts V_{in} = +0.4 volts	I_{CEX}	max. typ.		0.05	30.0 2.0	μa μa
fan-out available each gate	Fo	min.	6	11	6	....
noise margin, worst case③	$\triangle V_n$	min.	0.85	0.55	0.25	volts
dynamic electrical characteristics for V_{cc} = +6.0 volts						
switching time (see figures 1 and 2)						
turn-on time	T_{on}	typ.	46	39	31	ns
turn-off time	T_{off}	typ.	18	19	21	ns
average switching time $(T_{on}+T_{off}) \div 2$	T_{avs}	typ. max.	32	28 38	26	ns ns
ring propagation delay time, see figure 11 (ring of five gates)	T_{rpd}	typ.	37	35	34	ns

① Limiting values beyond which the serviceability of the device may be impaired.
② These terminals must not be biased negatively with respect to ground.
③ Minimum noise margin is given by: $V_{in}/1 - V_{CE(SAT)}$, where $V_{in}/1$ is the maximum input voltage for a 1-state output, and $V_{CE(SAT)}$ is the maximum output voltage in the 0-state at rated fan-out (6 or 11).

switching time test circuit and waveforms

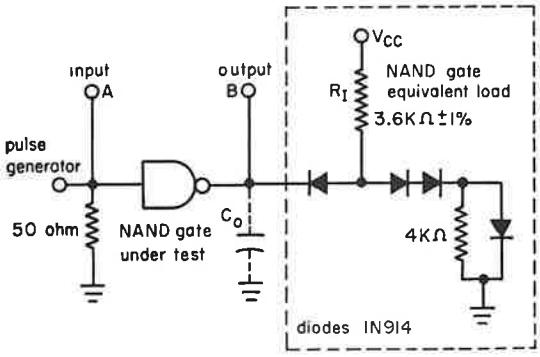


figure 1: Total capacitance C_o is 10 pf which includes test jig and scope probe. Unused inputs are open circuited.

figure 2: Average switching time: $T_{avs} = \frac{T_{on}+T_{off}}{2}$

Input pulse is 15 ns rise and fall, 500 ns width, 2 volt amplitude, and 20 kc repetition rate.

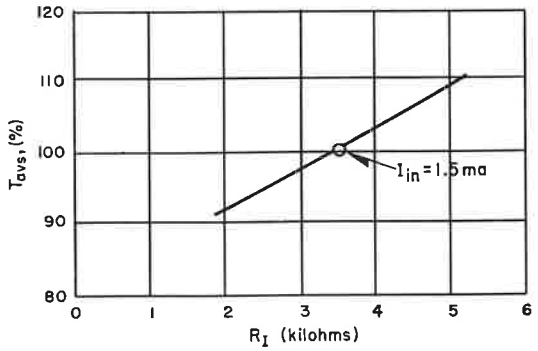
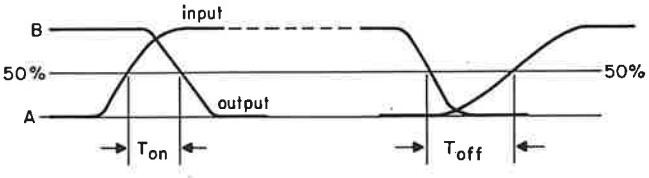


figure 3: Change in T_{avs} vs. input resistor value R_I at 25°C.



typical electrical characteristics

output and input current vs. temperature and supply voltage

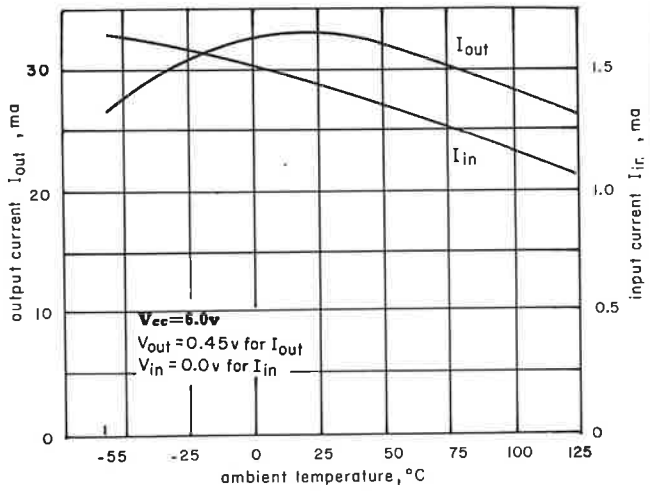


figure 4

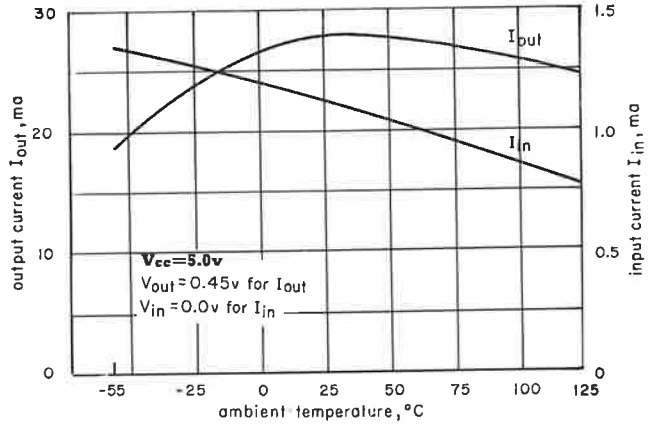


figure 5

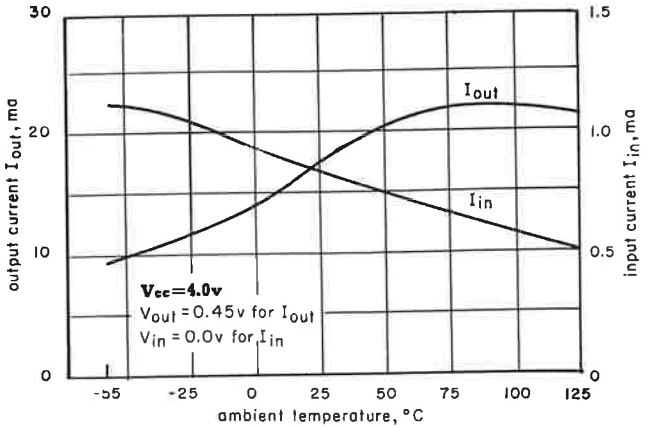


figure 6

output saturation characteristic vs. temperature

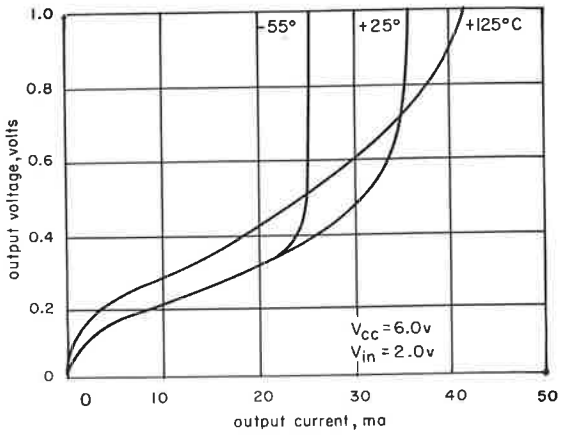


figure 7

output voltage vs. input voltage and temperature

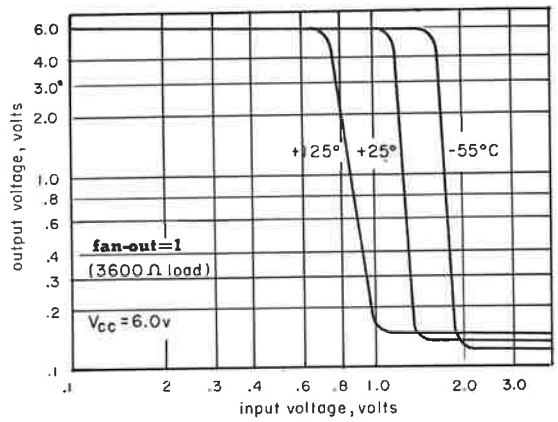


figure 8

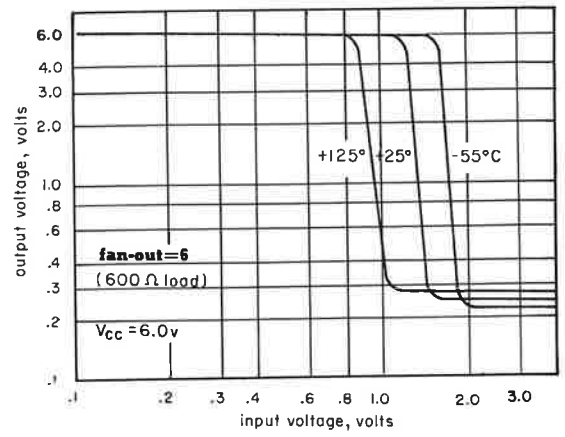


figure 9

typical electrical characteristics

power consumption (50% duty cycle)

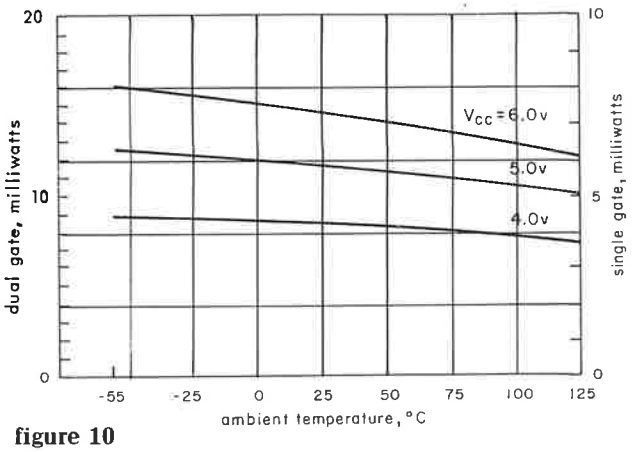


figure 10

ring propagation delay time vs. supply voltage and temperature

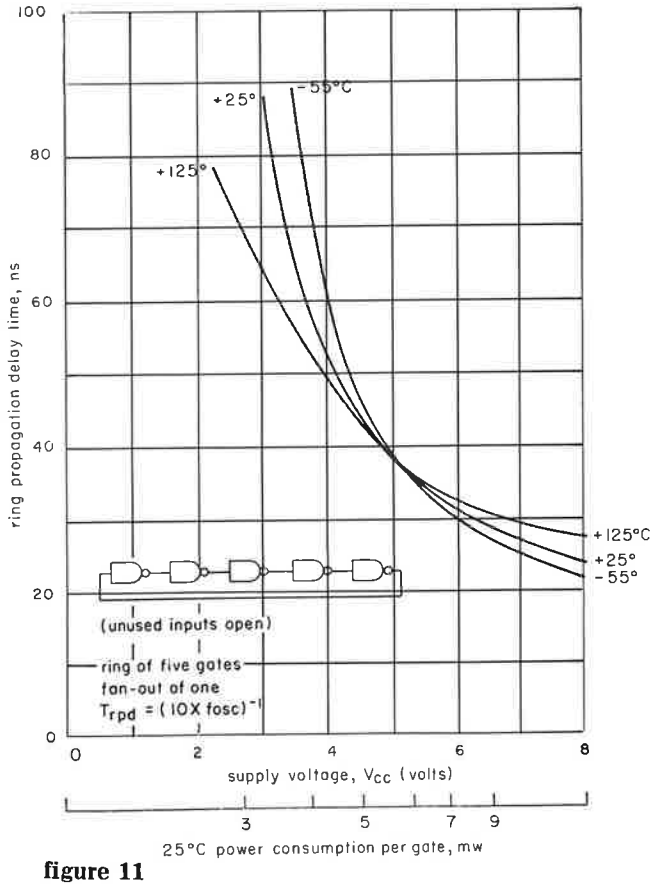


figure 11

fan-out test circuit (all integrated gates)

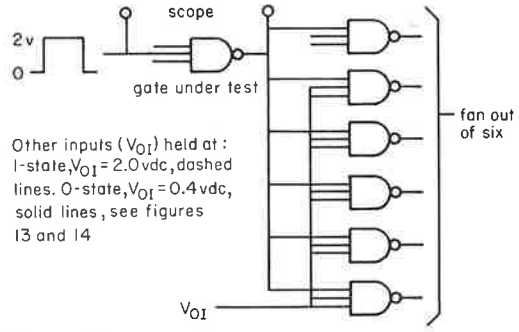

scope
2v
0
gate under test
fan out of six
Other inputs (V_{OI}) held at: 1-state, V_{OI} = 2.0 vdc, dashed lines. 0-state, V_{OI} = 0.4 vdc, solid lines, see figures 13 and 14
V_{OI}

figure 12

propagation time vs. fan-out

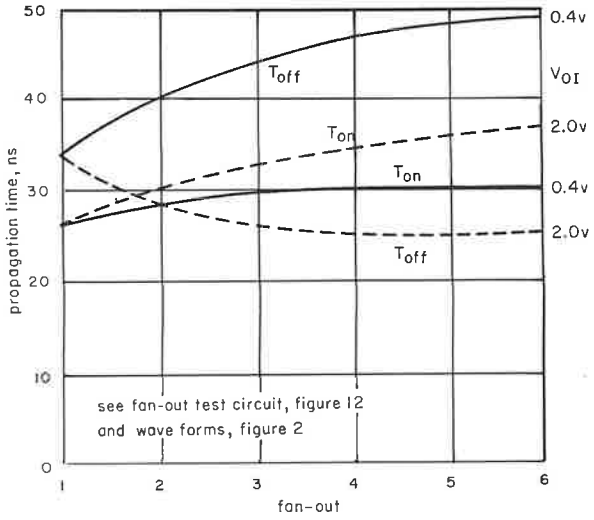


figure 13

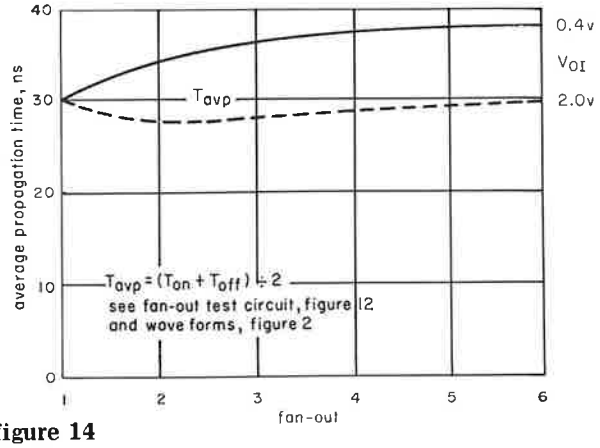


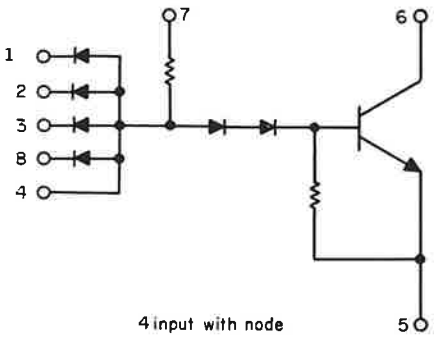
figure 14

schematic diagrams and pin numbering

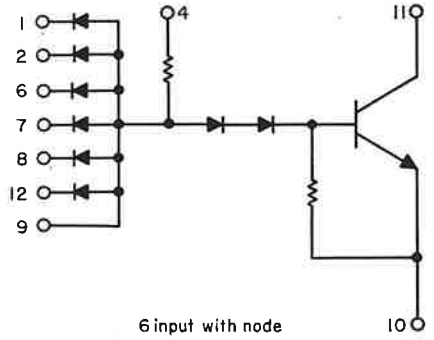
Suffix letters denote package, see page 6 for dimensions.

T package

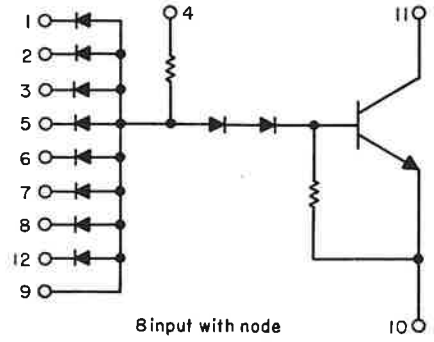
WM 204T (8 pin)



WM 214T (12 pin)

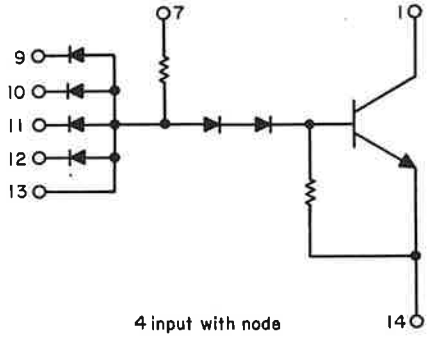


WM 224T (12 pin)

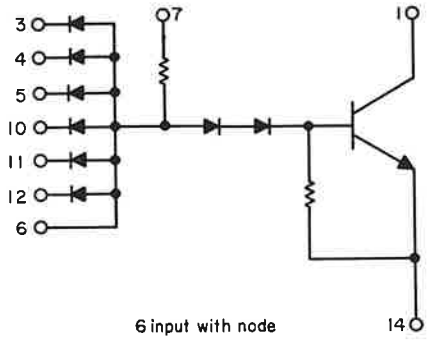


G package

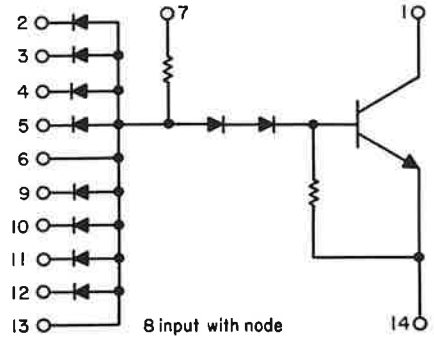
WM 204G



WM 214G

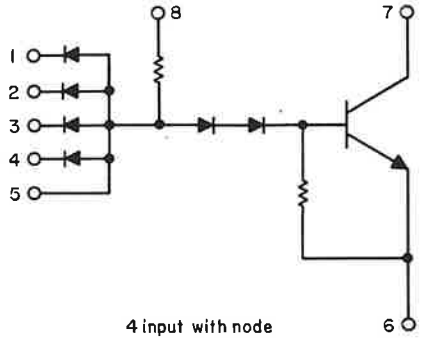


WM 224G

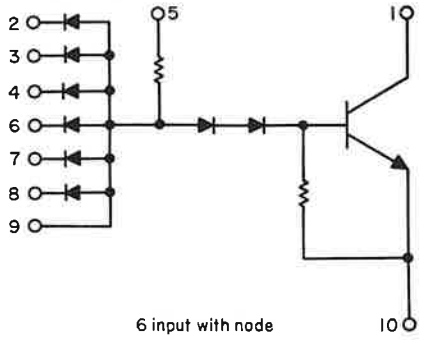


Q package

WM 204Q



WM 214Q

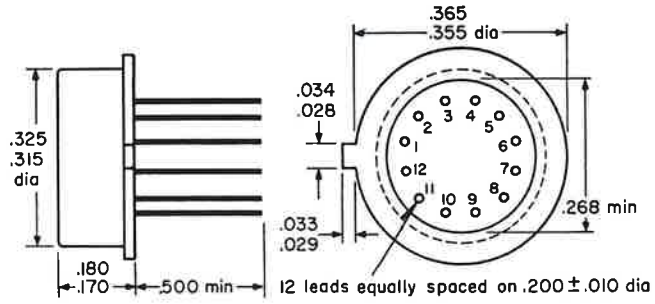


Package terminals not shown on circuit schematics (e.g. 3 and 5 on WM 214T) are unused; they are not connected to the circuit nor to the package.

single DTL NAND gates

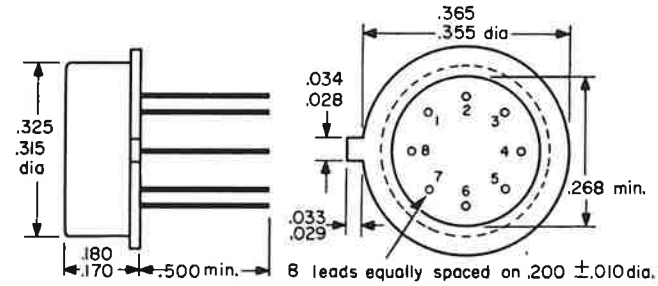
mechanical characteristics

T package—12 pins • 1.1 grams (typical)



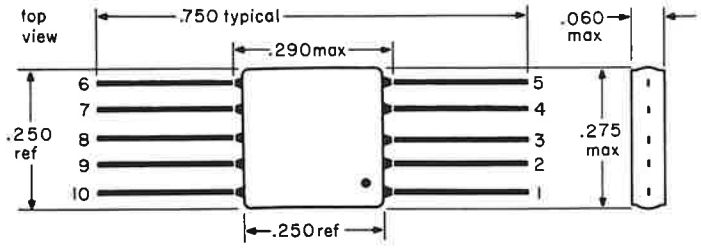
12 lead $\frac{.016}{.019}$ diameter gold plated KOVAR

T package—8 pins • 1.05 grams (typical)



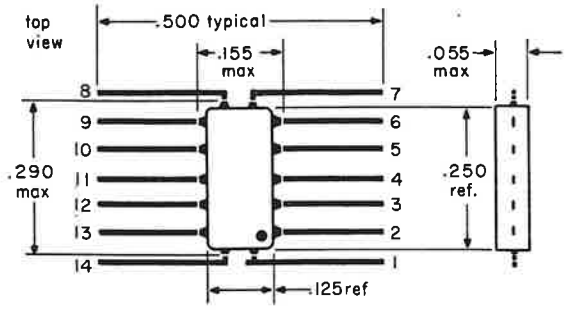
8 lead $\frac{.016}{.019}$ diameter gold plated KOVAR

Q style FLAT-PAK • 0.25 grams (typical)



Gold plated Kovar® leads are 15 x 5 mils on 50 mil centers.

G style FLAT-PAK • 0.1 grams (typical)

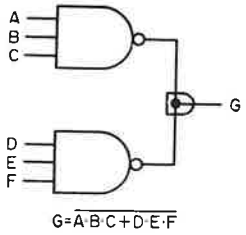


Gold plated Kovar leads are 12 x 4 mils on 50 mil centers. Base of package is ceramic. Lid is gold plated Kovar.

typical application

(logic symbols per ASA Y 32.14—1962)

AND-OR-NOT function



By connecting the output terminals of the two gates together, two levels of logic are accomplished in one gate switching time. The AND-OR-NOT logic function results (see logic diagram).

further information

condensed catalog 91-000

prices: section 91-120